IEEE P1581 Enhancements/Status

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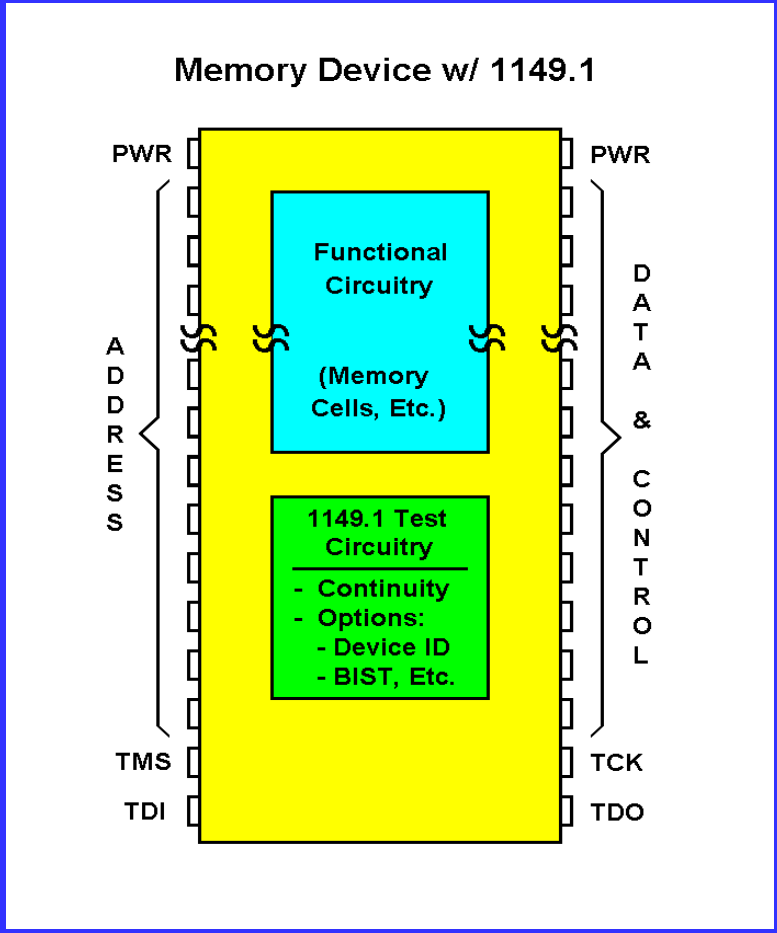
P1581 Working Group may or may not agree with content.

RJR BTW 17 SEP 2008

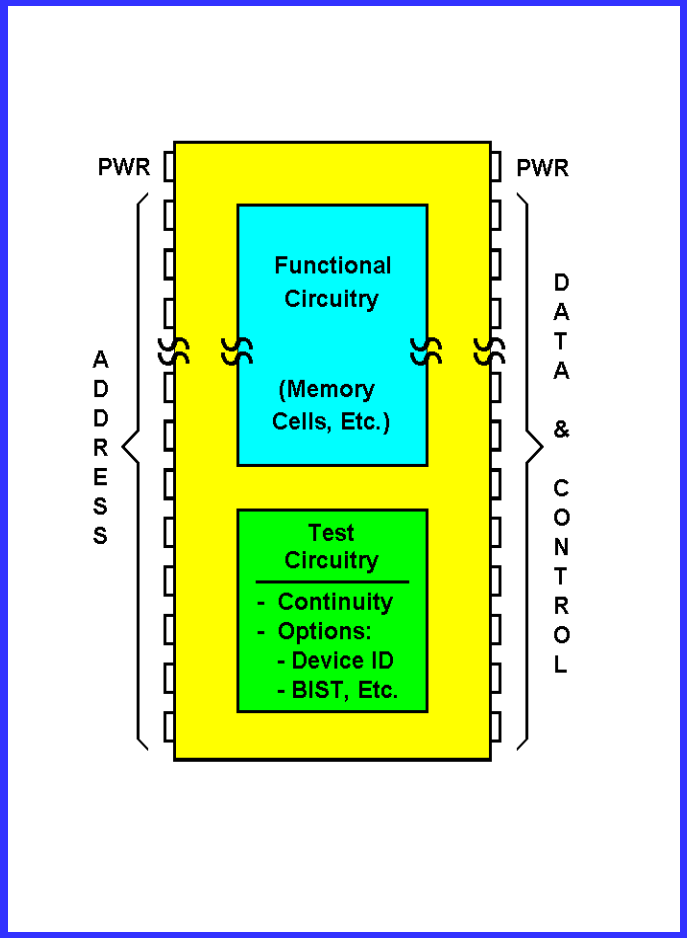
Outline

- P1581 Refresher
- Emulation Results & Status
- Simulation Results
- Future Plans

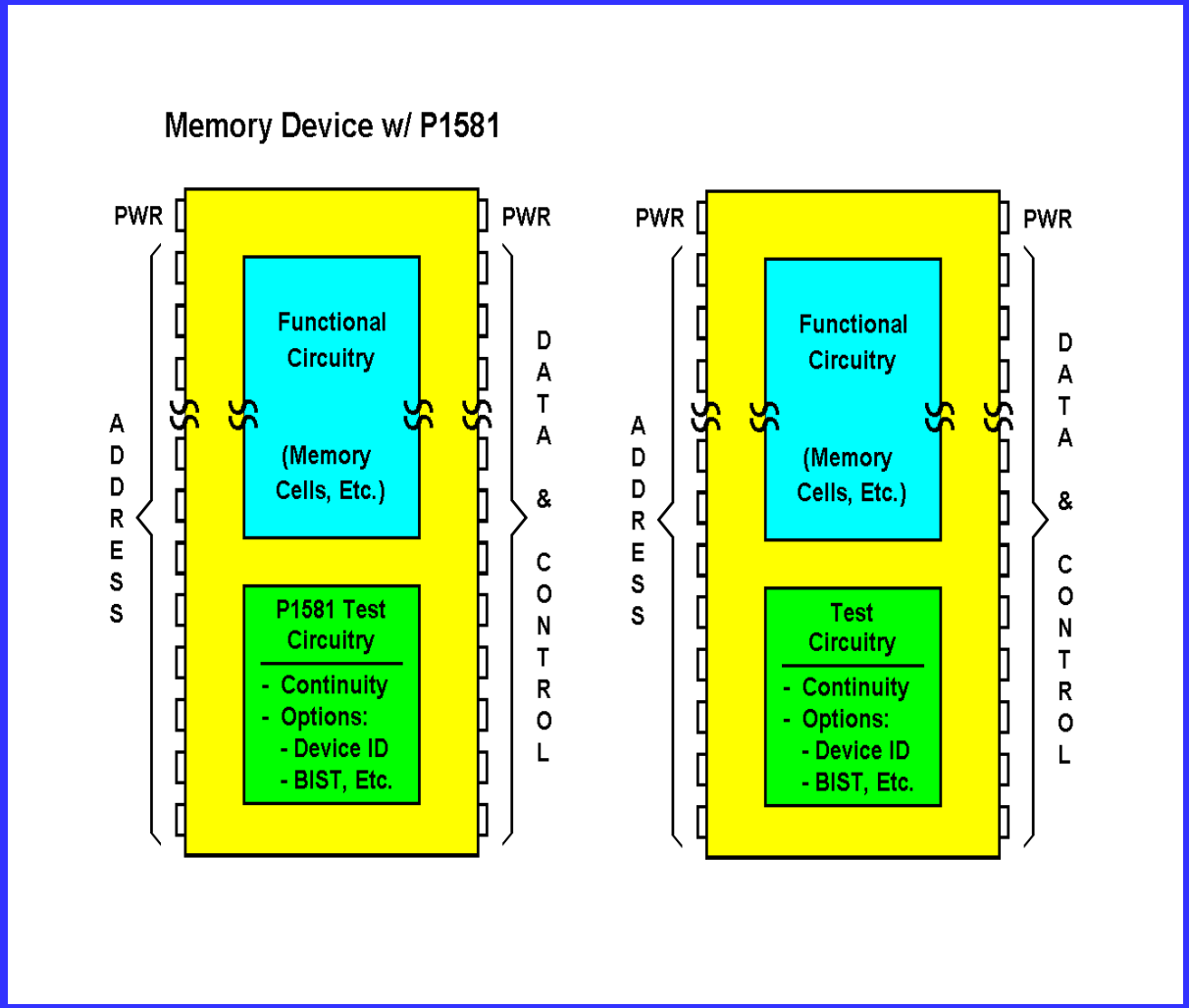
1149.1 Problem



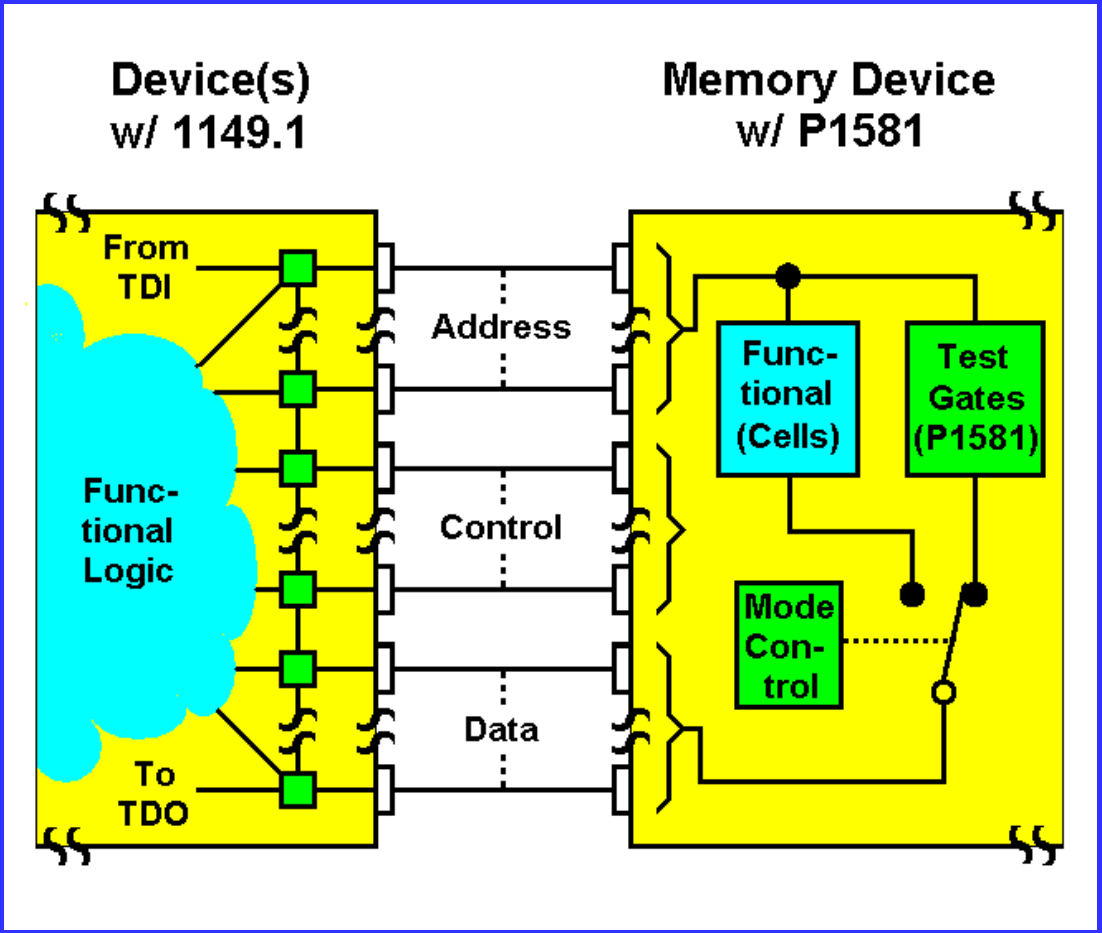
Ideal Solution



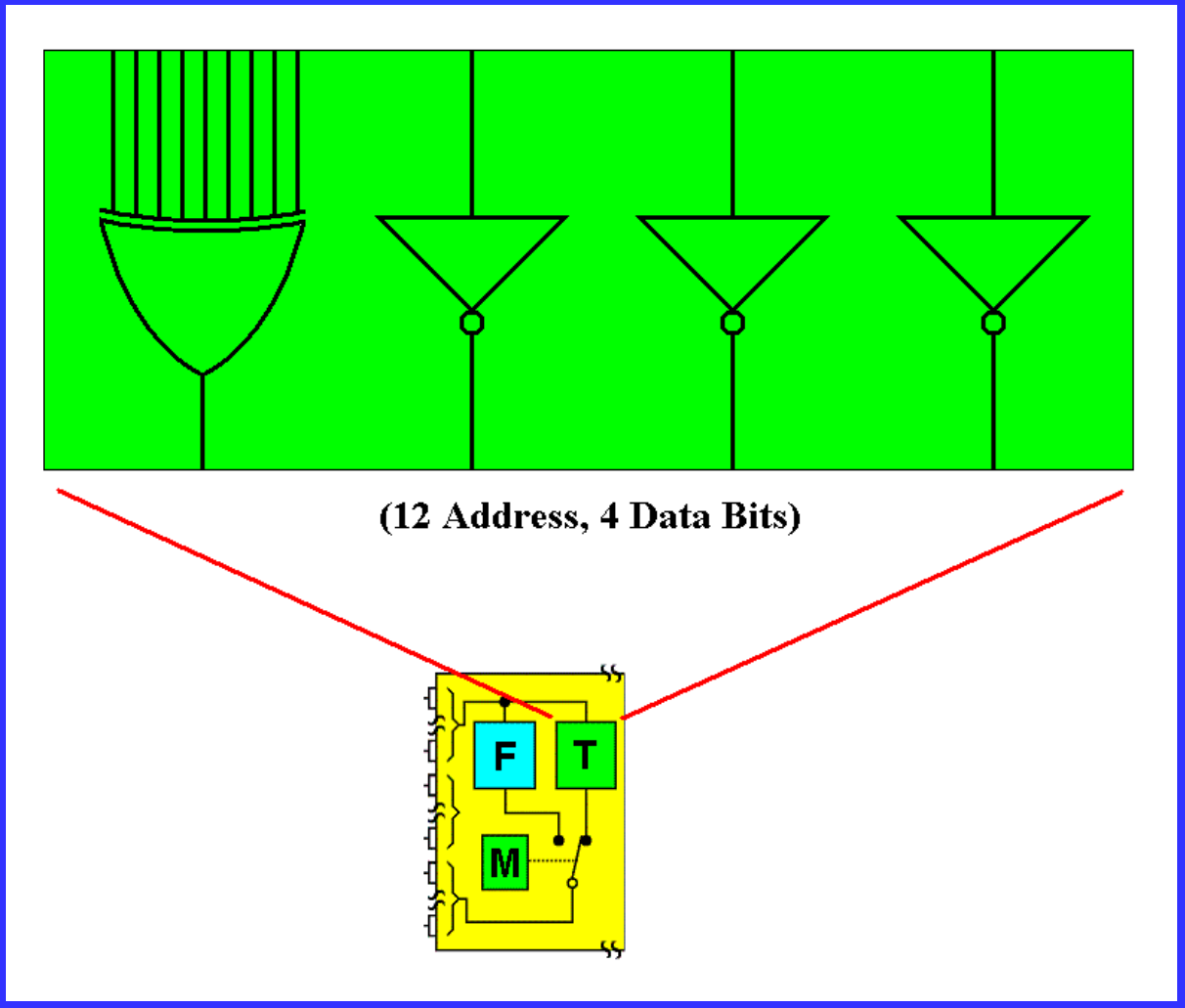
P1581 Vs. Ideal



P1581 Continuity Test Concept



Continuity Test Gating - IAX



Test Pattern Partitioning

12 Address Bits

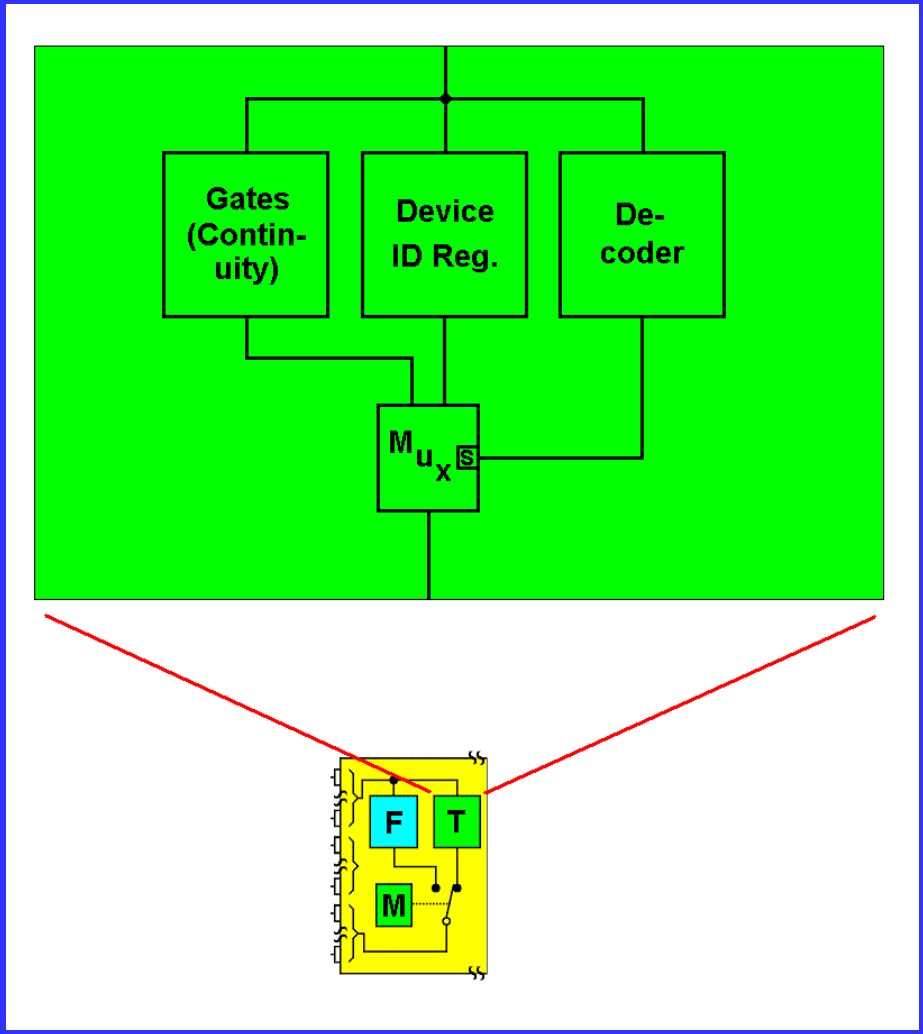
Unpartitioned

XXXXXXXXXXXX	4096	Continuity

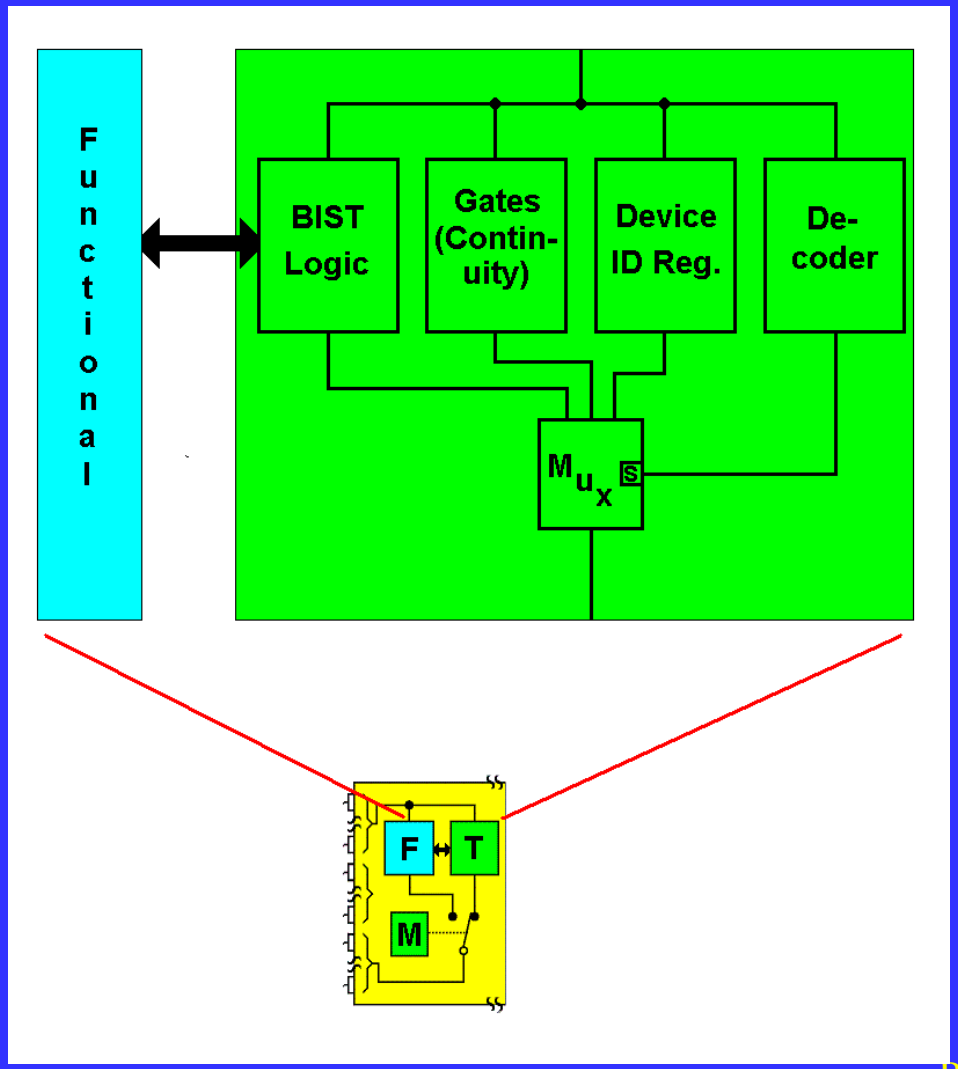
Partitioned

All 0's/1's	2	Continuity
One 0/1	24	" " "
Two 0's/1's	132	" " "
1110000XXXXX	32	Device ID
101010XXXXXX	64	Public
010101XXXXXX	64	Private

Device Identification Option



BIST & Device ID Options

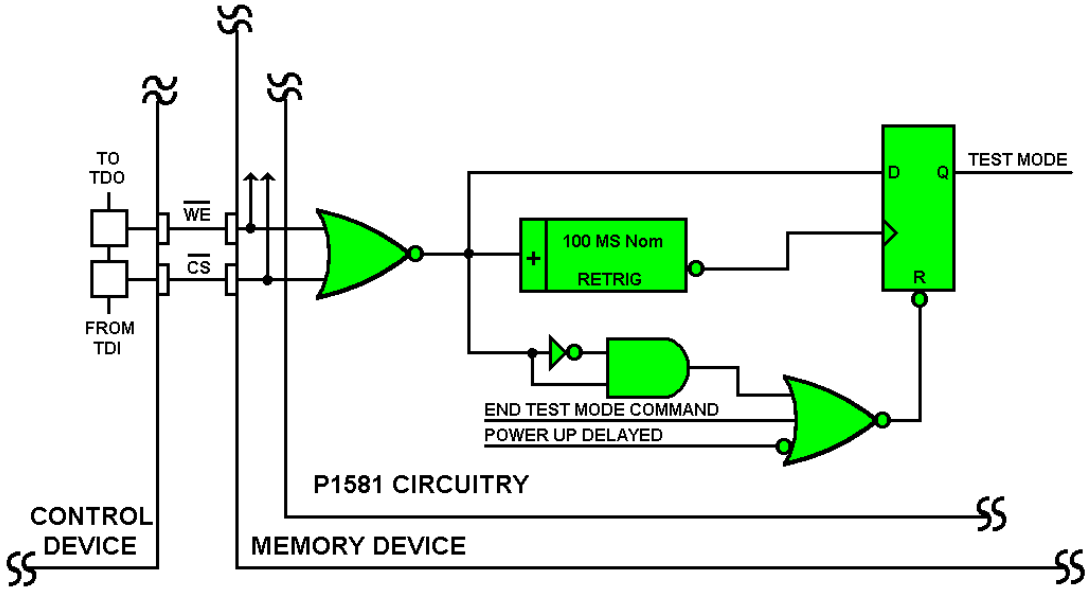


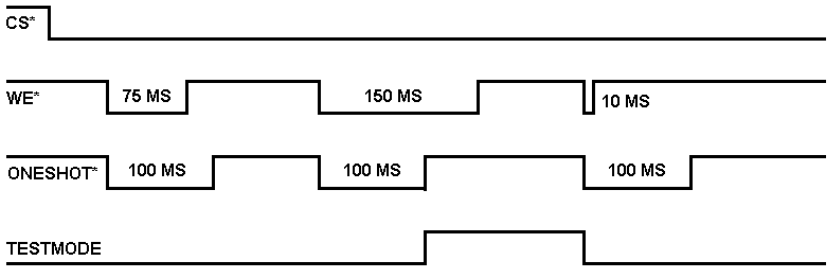
Test Mode Entry / Exit Options

Test Mode Entry & Exit Methods		
Acronym	Method	Description of Test Mode Control
Independent of Time After Powerup		
NFS	Non-Functional Stimulus	Device inputs driven by stimulus not possible in functional operation, but easily accomplished during boardtest operations (e.g., boundary scan, ICT, board level BIST).
CKF	Clock Frequency	Device clock input frequency altered (e.g., static) by board level control of the clock driver device.
CDE	Code Selection	Device codes not required for functional operation (e.g., read, write) are assigned to testmode control.
ANL	Analog Level	One or more device inputs are driven to a non-logical level for a duration not possible during functional operation.
TPN	Testpin	A dedicated device input is used for test mode control.
Initial Dependence on Powerup Timing		
PST	Powerup Selection	A short delay after powerup certain device inputs are monitored for presence of states that would be avoided through customary board design (e.g., write and chip select both active). Variousexit means.
PDT	Powerup Default	Test mode occurs at powerup. Exit occurs at beginning of first write unless other exit means chosen.

Summary of Test Mode Entry/Exit Methods.

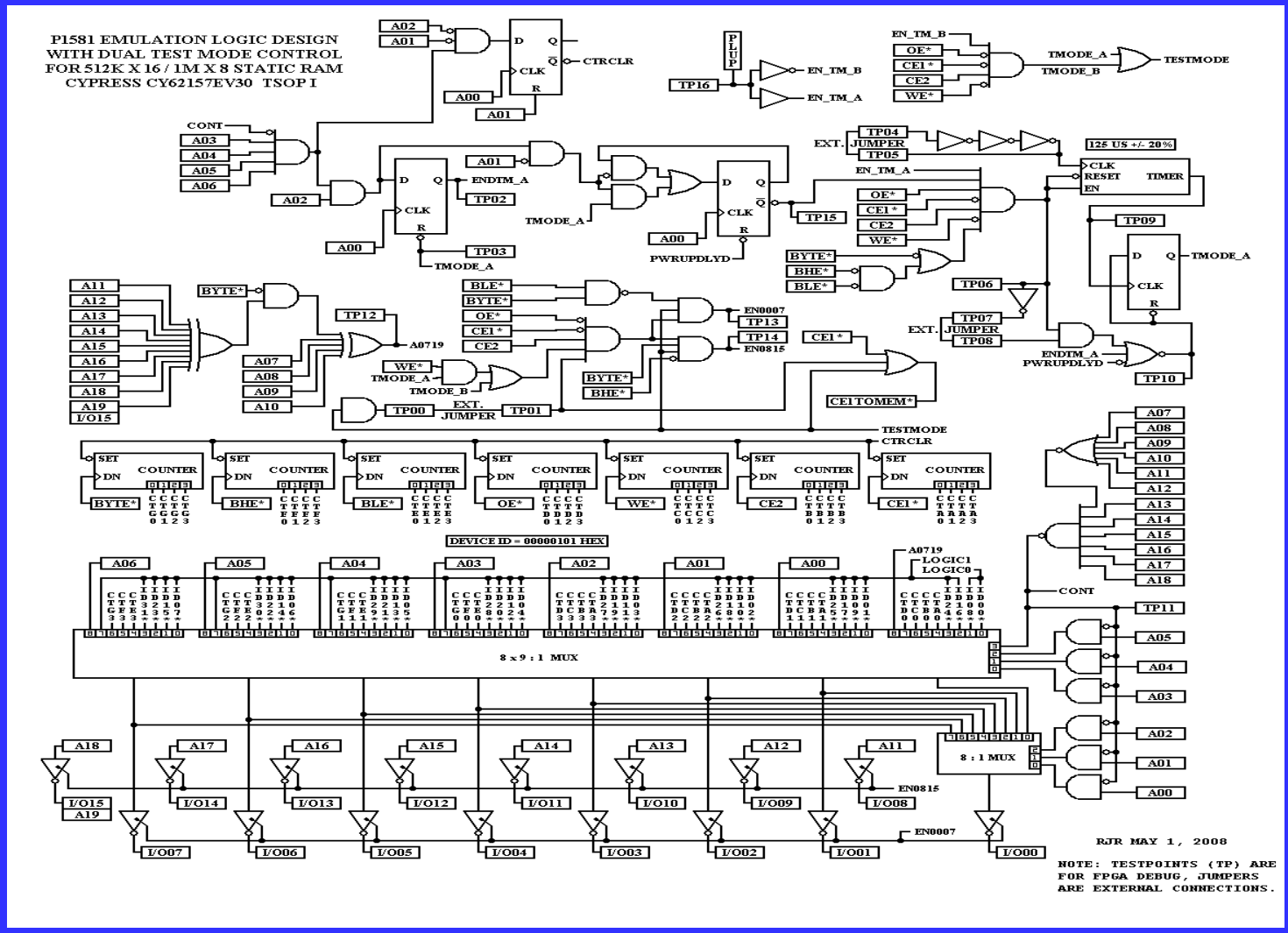
Non-Functional Stimulus Mode Control





Test Mode Control from Existing PCB BScan Circuitry
(No additional DFT)

NFS For Memory with I/O Pins



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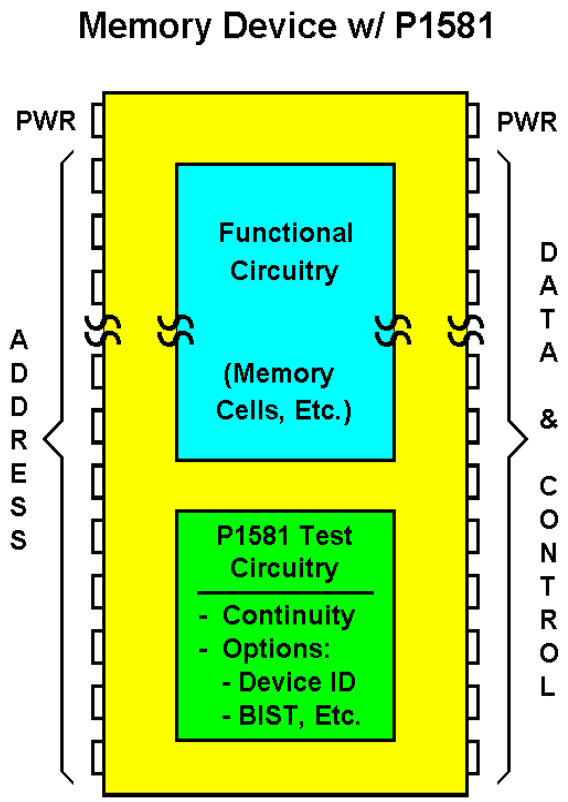
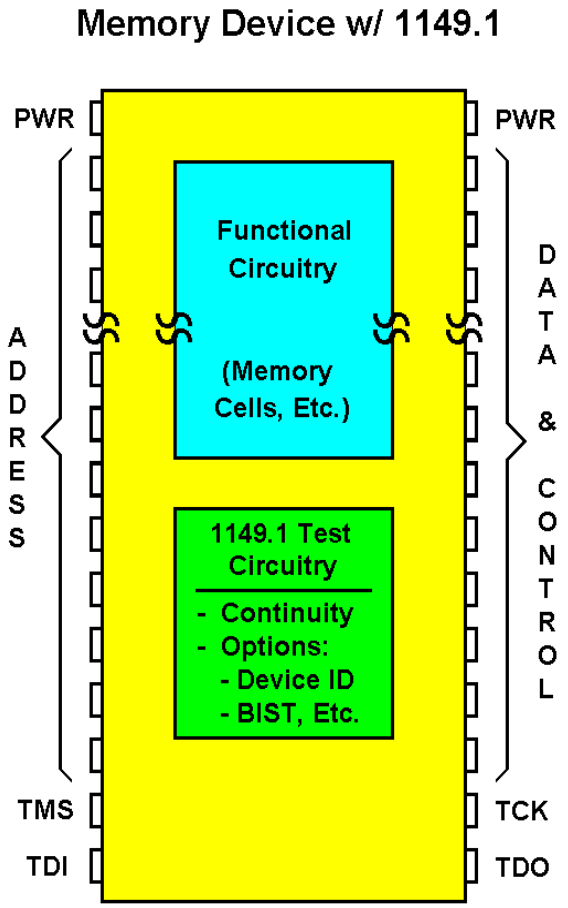
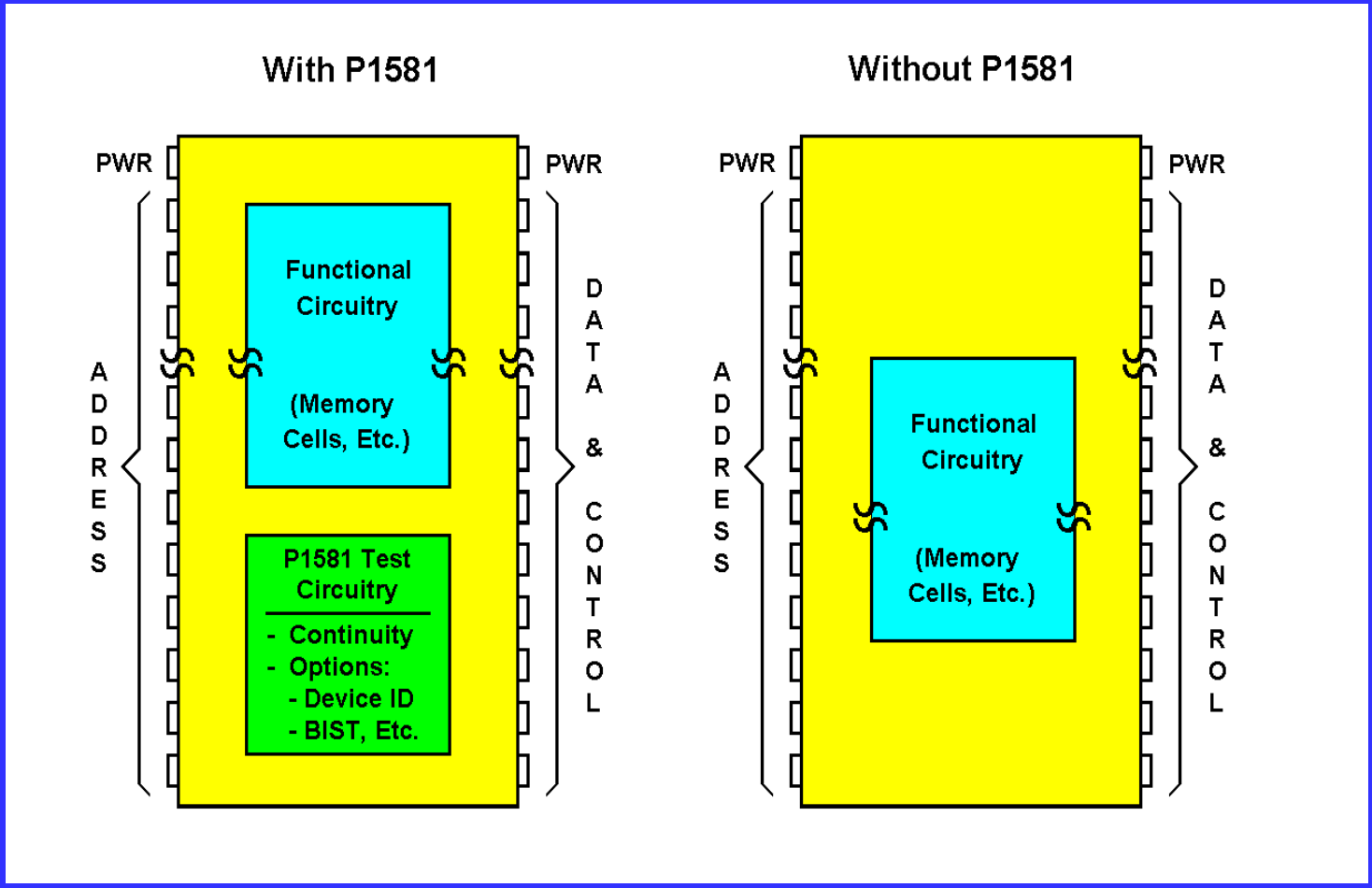
P1581 Vs. 1149.1





Comparison of Features - P1581 vs. 1149.1

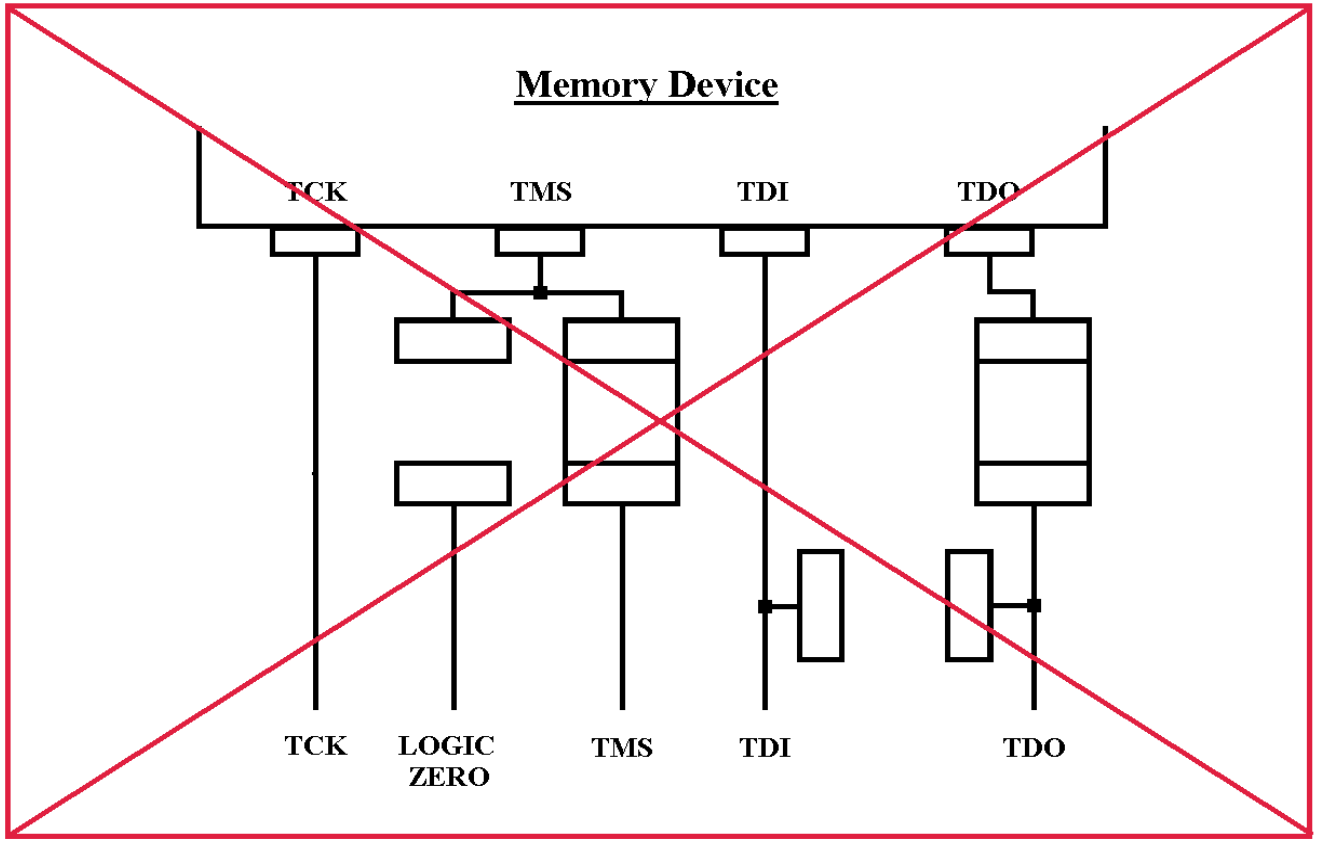
Legacy Compatibility (Transparency)



Emulation Benefits

- Proof of Concept
- “First Silicon Success” for New / Revised Memory Devices
- Test Tool Development
  - BScan Testers
  - ICT
  - Device Testers
- Test Code Development

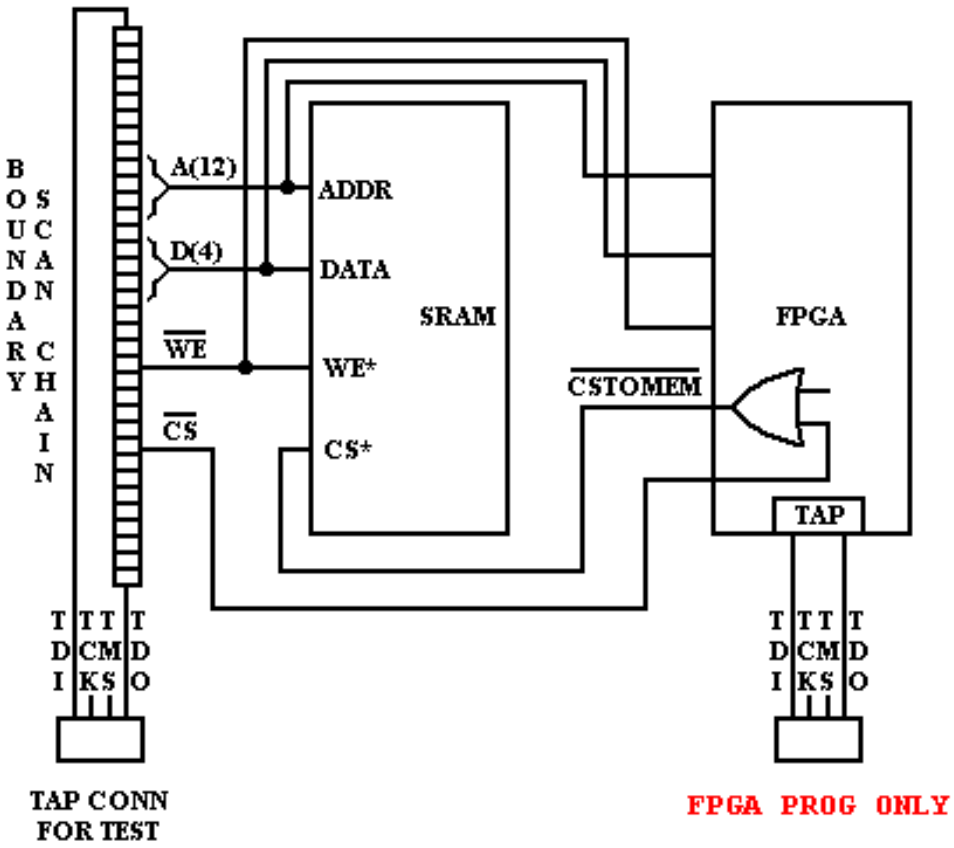
Emulation Benefits (cont.)



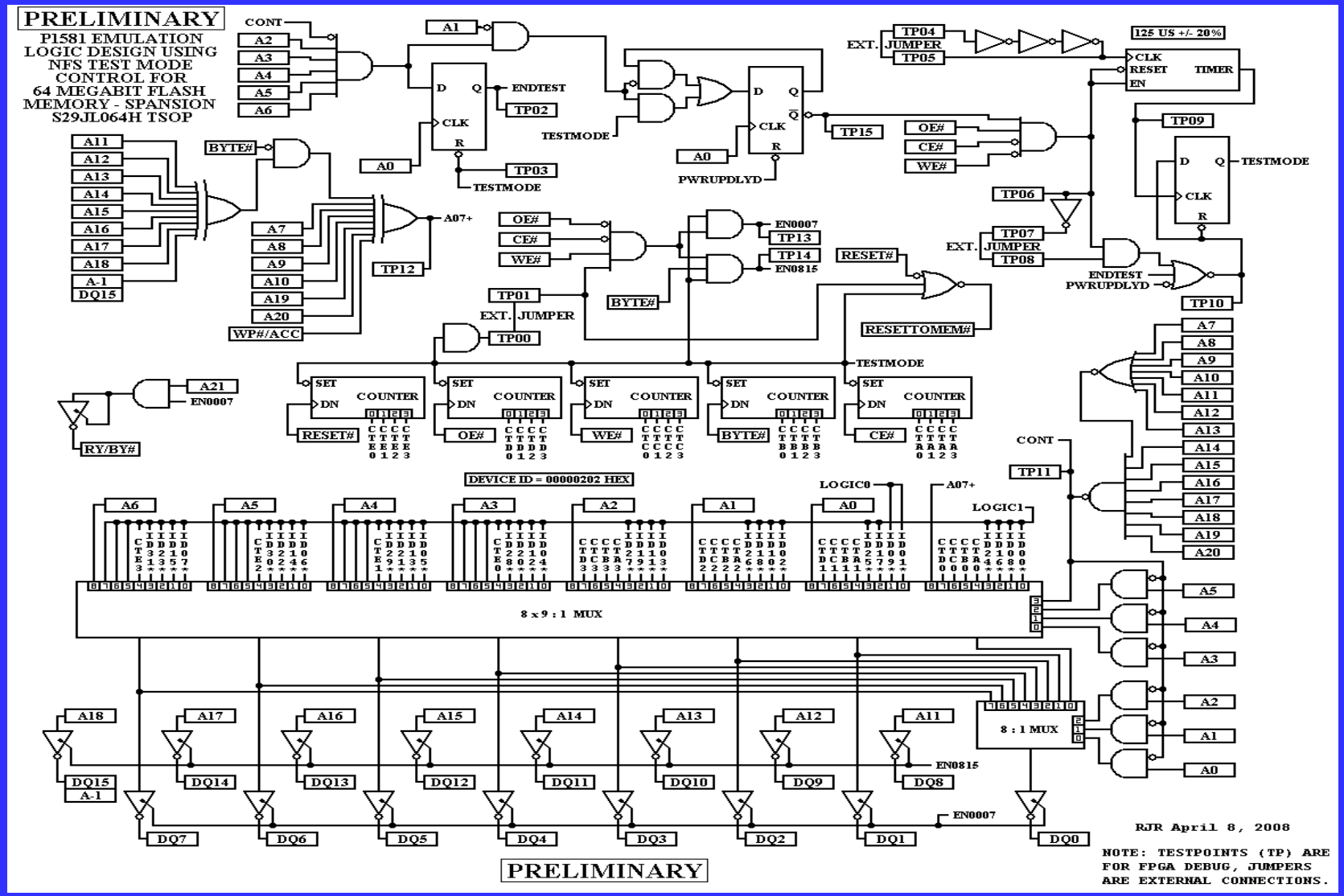
Emulation Status

- SRAM – Done / Demo @ BTW
- FLASH – Done / Demo @ BTW
- DRAM – In Design (Goepel Hardware Ready)

P1581 Emulation Concept



FLASH Emulation



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Simulation Results - SRAM

- Alcatel-Lucent Test Bench Simulator
- Michele Portolan / Brad Van Treuren
- Used Standard Model of Emulated SRAM
- No Problems Found
- Proved No Data Lost During Board Functional Write Operation to a P1581 Memory Device Inadvertently Left in Test Mode. (Test Mode Terminates.)
- March 2008

Working Group Future Plans

- Memory Device Manufacturer Involvement
- D I T T O ! ! ! ! ! ! !
- DRAM Emulation Completion for ITC Demo
- Simulate P1581 DRAM Device
- Develop Description Language
- Recruit an Editor
- Complete Draft and Ballot

Conclusion

- P1581 Includes Key 1149.1 Features
- Emulation Facilitates First Silicon Success
- P1581 Preferable to 1149.1 for Some Memory Devices

Further Information

- IEEE P1581 Working Group Website:
  http://grouper.ieee.org/groups/1581/
- Sit In on WG Phone Conference – Oct. 10, 10:30 EDT
- Contact Author: r.russell@ieee.org
- Discuss This Evening w/ H. Ehrenberg
- Common Questions Part of Presentation Thursday